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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,563	06/03/2005	Hisaharu Nakahara	NAA218	4547

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GALLAGHER & LATHROP, A PROFESSIONAL CORPORATION
601 CALIFORNIA ST
SUITE 1111
SAN FRANCISCO, CA 94108

EXAMINER	
NATALINI, JEFF WILLIAM	

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 10/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/537,563	NAKAHARA, HISAHARU	
	Examiner	Art Unit	
	Jeff Natalini	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *4-6,8 and 9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/3/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of the species of figure 3, claims 1-3 and 7 in the reply filed on 9/26/06 is acknowledged. Accordingly, claims 4-6, 8, and 9 have been withdrawn from consideration.

The election requirement is hereby repeated and made FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takechi et al. (US Pub 20020171446) in view of De Wolf et al. (3772595).

Takechi et al. discloses a voltage-impressed current measuring apparatus which impresses a prescribed voltage and measures the current flowing to a load apparatus (abstract) comprising

a current-range switching portion (figure 1) connecting in series a current buffer with switches (figure 1 element 29), having output stages capable of being electrically connected or disconnected in response to a supplied control signal (figure 1, I/O control signal), and current measurement resistances of resistance values respectively

connected to the output stages of the current buffers with switches (figure 1, element 23), when the switch is connected in the buffer the output receives the waveform (fig 1);

a direct-current power supply portion, supplying a prescribed direct-current voltage to said load apparatus through the series connection of the current buffer with switch (figure 1, test waveform; also seen in figure 2-Vcc, and figure 8, voltage generator) and current measurement resistance selected by said current range switching means (the switching means SW1 determines when the waveform is applied);

and a potential difference measuring means, measuring, as a value corresponding to the current flowing in said load apparatus, the potential difference across the two ends of the current measurement resistance of said series connection due to the current which accompanies the impression of said direct-current voltage on said load apparatus and flows from the current buffer with switch of said selected series connection to said load apparatus (figure 1, elements 21 and 27 with a comparative voltage; see paragraphs 27 and 28 pg 2).

Takechi et al. lacks wherein a plurality of pairs are connected in series of current buffers with switches wherein the resistance values are difference for each of the stages, wherein any one of the pairs is selected by a control signal to switch the current measurement range said output stage of the current buffer with switch of said selected pair taken to be in a connected state.

De Wolf et al. discloses a current sensing device (abstract) wherein a plurality of pairs are connected in series of current buffers (figure 1 elements 16, 18, and 20) with switches (figure 1 elements 22, 24, and 26) to the load device (figure 1 element 28),

wherein any one of the pairs is selected by a control signal to switch the current measurement range said output stage of the current buffer with switch of said selected pair taken to be in a connected state (col 4 line 29-43).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Takechi et al. to include the teachings of De Wolf et al. of a plurality of pairs connected in series with the switches/buffers, where each of the pairs is controlled by a control signal to transfer a proper signal to the load device as taught by De Wolf et al. and when combining these two references in order to produce a different value to the load, the resistance after the buffer of Takechi et al. would have to be different for each of the plurality of switch/buffer combinations, in order to provide varied output load conditions under which the device can be tested (col 4 line 26-28).

4. Claims 2, 3, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takechi et al. (US Pub 20020171446) in view of De Wolf et al. (3772595) as applied to claim 1 above, and further in view of Hirofumi (JP 63-082377 on IDS).

Tackechi et al. discloses:

(claim 3) wherein the output side voltage of said current measurement resistances and the input side with the reference values are supplied to said potential differences measuring portion (fig 1 elements 21 and 27 and paragraph 28 pg 2).

Takechi et al. as modified lacks:

(claim 2) the power supply comprises a digital to analog converter and an operational amplifier which controls by feedback the voltage impressed on said load

apparatus with respect to said reference voltage and supplies the impressed voltage to said load apparatus via said range switching portion,

(claim 3) wherein the plurality of current buffers are connected to the output side of the operation amplifier, the resistances are mutually connected and the input side voltage of the current buffers with switches; and

(claim 7) wherein said current power supply portion comprises a first resistance inserted between the output of said digital to analog converter and the inverted input of said operational amplifier, and a second resistance inserted in the feedback path from said load apparatus to the inverted input of said operational amplifier, and the non-inverter input of said operational amplifier is connected to ground.

Hirofumi discloses a current measuring circuit:

(claim 2) the power supply comprises a digital to analog converter (figure 1 element 16) and an operational amplifier (fig 1 element 14) which controls by feedback (fig 1, feedback seen in elements 22 and 24) the voltage impressed on said load apparatus with respect to said reference voltage and supplies the impressed voltage to said load apparatus (fig 1 element 10) via said range switching portion (fig 1 elements Ry1-Ryn),

(claim 3) wherein the plurality of current buffers are connected to the output side of the operation amplifier (fig 1 element 14), the resistances are mutually connected and the input side voltage of the current buffers with switches (fig 1 elements R1-Rn and Ry1-Ryn); and

(claim 7) wherein said current power supply portion comprises a first resistance (fig 1 element 20) inserted between the output of said digital to analog converter (fig 1 element 16) and the inverted input of said operational amplifier (fig 1 element 14), and a second resistance (fig 1 element 24) inserted in the feedback path from said load apparatus (fig 1 element 10) to the inverted input of said operational amplifier (fig 1 element 14), and the non-inverter input of said operational amplifier is connected to ground (fig 1 element 14 has non-inverted input connected to ground).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Takechi et al. to include a digital to analog converter in the power supply and an operational amplifier with a ground input to the non inverting input and a resistor between the D/A converter and the inverting input of the operational amplifier with a feedback loop connecting the input to the load element as taught by Hirofumi in order to provide a quick current measurement (see purpose in English abstract).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ryder (3978402) discloses an apparatus for producing an electrical output signal whose magnitude is linearly representative of the value of an unknown resistance. Persons (5521493) discloses a semiconductor test system include a driver/load circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Natalini whose telephone number is 571-272-2266. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Hirshfeld can be reached on 571-272-2168. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeff Natalini

SUPERVISORY PATENT EXAMINER